AMENDMENTS TO THE CLAIMS:

Please amend claims 21-23, 27-29, 33-35 and 39-41.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1-20 (canceled)

Claim 21 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on the other surface of said wiring substrate, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said wiring substrate having ~~a number of~~ at least one through-hole set comprising at least two through-holes formed in conforming relationship with said at least two chip electrodes; and

~~a number of bumps~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed ~~respectively~~ in any one of said at least two through-holes of said wiring substrate ~~in conforming relationship with said at least two chip electrodes~~ and electrically connecting between said common wiring of said wiring substrate ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 22 (currently amended): A semiconductor device comprising:

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a wiring substrate having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on the other surface of said wiring substrate, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said wiring substrate is bent at at least one position;

said wiring substrate having ~~a number of~~ at least one through-hole set comprising at least two through-holes formed in conforming relationship with said at least two chip electrodes; and

~~a number of bumps~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed ~~respectively~~ in any one of said at least two through-holes of said wiring substrate ~~in conforming relationship with said at least two chip electrodes~~ and electrically connecting between said common wiring of said wiring substrate ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 23 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on the other surface of said wiring substrate, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two

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chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said wiring substrate has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having ~~a number of~~ at least one through-hole set comprising at least two through-holes; and

~~a number of bumps~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed ~~respectively~~ in any one of said at least two through-holes of said wiring substrate ~~in conforming relationship with said at least two chip electrodes~~ and electrically connecting between said common wiring of said wiring substrate ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 24 (previously presented): A semiconductor device according to claim 21, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 25 (previously presented): A semiconductor device according to claim 22, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 26 (previously presented): A semiconductor device according to claim 23, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 27 (currently amended): A semiconductor device comprising:

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a wiring substrate having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on said one surface of said wiring substrate, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged from an edge of said semiconductor chip toward its inner side; and

~~a number of bumps disposed~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed on said ~~wiring~~ one surface of said wiring substrate ~~respectively~~ in conforming relationship with any one of said at least two chip electrodes and electrically connecting between said common wiring of said wiring substrate ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 28 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of ~~working~~ wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on said one surface of said wiring substrate and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said wiring substrate~~, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said wiring substrate is bent at at least one position; and

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~~a number of bumps disposed~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed on said one surface of said wiring substrate ~~respectively~~ in conforming relationship with any one of said at least two chip electrodes and electrically connecting between said common wiring of said wiring substrate ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 29 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on said one surface of said wiring substrate, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said wiring substrate has an end width larger than an inter-electrode distance between said chip electrodes; and

~~a number of bumps disposed~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed on said one surface of said wiring substrate ~~respectively~~ in conforming relationship with any one of said at least two chip electrodes and electrically connecting between said common wiring of said wiring substrate ~~with~~ and said at least two chip electrodes,

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wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 30 (previously presented): A semiconductor device according to claim 27, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 31 (previously presented): A semiconductor device according to claim 28, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 32 (previously presented): A semiconductor device according to claim 29, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 33 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on the other surface of said TAB tape, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having ~~a number of~~ at least one through-hole set comprising at least two through-holes formed in conforming relationship with said at least two chip electrodes; and

~~a number of bumps~~ at least one bumps set comprising at least two pairs of bumps, each pair of which is formed ~~respectively~~ in any one of said at least two through-holes of said TAB

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tape ~~in conforming relationship with said at least two chip electrodes~~ and electrically connecting between said common wiring of said TAB tape ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 34 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on the other surface of said TAB tape, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said TAB tape is bent at at least one position;

said TAB tape having ~~a number of~~ at least one through-hole set comprising at least two through-holes formed in conforming relationship with said at least two chip electrodes; and

~~a number of bumps~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed ~~respectively~~ in any one of said at least two through-holes of said TAB tape ~~in conforming relationship with said at least two chip electrodes~~ and electrically connecting between said common wiring of said TAB tape ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 35 (currently amended): A semiconductor device comprising:

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a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on the other surface of said TAB tape, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said TAB tape has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having ~~a number of~~ at least one through-hole set comprising at least two through-holes formed in conforming relationship with said at least two chip electrodes; and

~~a number of bumps~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed ~~respectively~~ in any one of said at least two through-holes of said TAB tape ~~in conforming relationship with said at least two chip electrodes~~ and electrically connecting between said common wiring of said TAB tape ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 36 (previously presented): A semiconductor device according to claim 33, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 37 (previously presented): A semiconductor device according to claim 34, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

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Claim 38 (previously presented): A semiconductor device according to claim 35, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 39 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on said one surface of said TAB tape, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged from an edge of said semiconductor chip toward its inner side; and

~~a number of bumps disposed~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed on said ~~wiring~~ one surface of said TAB tape ~~respectively~~ in conforming relationship with any one of said at least two chip electrodes and electrically connecting between said common wiring of said TAB tape ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 40 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on said one surface of said TAB tape, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes

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~~in a~~ connected to said common wiring layer, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said TAB tape is bent at at least one position; and

~~a number of bumps disposed~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed on said ~~wiring~~ one surface of said TAB tape ~~respectively~~ in conforming relationship with any one of said at least two chip electrodes and electrically connecting between said common wiring of said TAB tape ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 41 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface, said wiring having a common wiring;

a semiconductor chip disposed on said one surface of said TAB tape, and having a common wiring layer and at least one chip electrode set comprising at least two chip electrodes ~~in a~~ connected to said common wiring layer ~~of said semiconductor chip~~, wherein said at least two chip electrodes are arranged parallel to an edge of said semiconductor chip and said common wiring of said TAB tape has an end width larger than an inter-electrode distance between said chip electrodes; and

~~a number of bumps disposed~~ at least one bump set comprising at least two pairs of bumps, each pair of which is formed on said ~~wiring of~~ one surface of said TAB tape ~~respectively~~ in conforming relationship with any one of said at least two chip electrodes and electrically

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connecting between said common wiring of said TAB tape ~~with~~ and said at least two chip electrodes,

wherein said at least two pairs of bumps each comprise a first bump and a second bump integrated with each other.

Claim 42 (previously presented): A semiconductor device according to claim 39, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 43 (previously presented): A semiconductor device according to claim 40, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 44 (previously presented): A semiconductor device according to claim 41, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 45 (previously presented): A semiconductor device according to claim 21, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 46 (previously presented): A semiconductor device according to claim 22, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 47 (previously presented): A semiconductor device according to claim 23, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

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Claim 48 (previously presented): A semiconductor device according to claim 27, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 49 (previously presented): A semiconductor device according to claim 28, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 50 (previously presented): A semiconductor device according to claim 29, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 51 (previously presented): A semiconductor device according to claim 33, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 52 (previously presented): A semiconductor device according to claim 34, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 53 (previously presented): A semiconductor device according to claim 35, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 54 (previously presented): A semiconductor device according to claim 39, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

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Claim 55 (previously presented): A semiconductor device according to claim 40, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 56 (previously presented): A semiconductor device according to claim 41, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

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